REMARKS

Claims 39-51 are pending in the present application. Claims 39, 43, and 48-51 have been amended. A marked-up version, showing changes made, is attached hereto as Appendix A. Reconsideration is requested in light of the amendments and following remarks.

Claims 39, 43, and 48 have been amended to positively recite an electro-mechanically polished layer "containing no hardening additive."

Claims 49, 50, and 51 have been amended to positively recite an electro-mechanically polished metal layer "consisting of a noble metal."

Claims 39, 43, and 48 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 40-42 and 44-47 are also rejected due to their dependency upon the rejected base claims. Claims 39, 43, and 48 have been amended to overcome the rejection. Accordingly, withdrawal of the rejection is solicited for claims 39-48.

Claims 39-47 and 49-50 stand rejected under 35 U.S.C. §102(b) as being anticipated over Kawakubo. Reconsideration is respectfully requested.

The cited reference fails to teach or suggest the present invention. As explained below, even if one used the CMP method disclosed in Kawakubo, one still would not achieve the same structure as recited in Applicants' claims.

The literature of record demonstrates that CMP and EMP are entirely different resulting in significant structural differences. In "Electrochemical Planarization for Multi-Level Metallization of Microcircuitry" by Anthony F. Bernhardt et al., disclosed in Applicants' IDS, "electrochemical planarization offers unique advantages over previous planarization techniques," including CMP and MP (Page 46, Col. 2). An EMP processed surface has structural uniformity "within two percent," across a wafer (Page 46, Col. 3 and FIGS. 9-10). This is a significant structural difference from a CMP or MP processed layer.

Further, Applicants' EMP layer contains no hardening additive and thus has a lower hardness than Kawakubo's layer. Kawakubo teaches that "[p]latinum, an example of a pure noble metal . . . is a soft metal having Vickers hardness of 40 or less." (Col. 6, lines 15-17), and that "it is necessary to add an appropriate element to noble metal (e.g., platinum)," so that the layer can withstand CMP (Col. 6, lines 24-29) (emphasis added). Kawakubo's structure comprises a bottom electrode with "a Vickers hardness of 80 or more" to withstand CMP or MP processes (Col. 6, lines 8-10). As is known in the art, CMP uses a mechanical downforce of at least 2-3 psi. EMP uses a downforce as minimal as 0.1 psi. Accordingly, metals containing no hardening additive, such as a pure noble metal (e.g., platinum), can form Applicants' claimed structure.

Claims 39, 43, and 48 have been amended to positively recite this structural difference. Claims 39, 43, and 48 recite an EMP layer "containing no hardening additive." (emphasis added). For at least these reasons, dependent claims 40-42 which incorporate all of the limitations of independent claim 39, and dependent claims 44-47 which incorporate all of the limitations of claim 43, are neither anticipated by, nor rendered obvious over Kawakubo.

Moreover, Kawakubo's metal layer specifically includes a hardening additive so that the metal layer can withstand CMP and MP processing (See Col. 6, lines 33-42). Again, Kawakubo's metal layer, which comprises at least a noble metal and an additive, is structurally different from Applicants' metal layer.

Claims 49-51 have been amended to positively recite this structural difference. Claims 49-51 recite an EMP processed layer "consisting of a noble metal." (emphasis added). Accordingly, claims 49-51 are neither anticipated by, nor rendered obvious over Kawakubo.

Claims 48 and 51 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kawakubo in view of Sandhu. Reconsideration is respectfully requested.

The arguments provided above regarding the rejection of claims 39-47 and 49-50 are equally applicable here. Specifically, electro-mechanically polished metal layers are structurally distinct from layers polished by CMP or MP taught in Kawakubo. Kawakubo's layer is much harder and comprises a hardening additive for structural rigidity. Sandhu is relied upon as disclosing a memory device electrically coupled to a processor and adds nothing of significance to the issue of EMP layers containing no hardening additive.

The cited references fail to suggest a "a processor . . . a memory device . . . comprising . . . a substrate, and a capacitor . . . comprising at least one electro-mechanically polished layer containing no hardening additive," as claim 48 recites (emphasis added), or a . "a processor . . . a memory device . . . comprising . . . a substrate, and a capacitor . . . comprising at least one electro-mechanically polished metal layer consisting of a noble metal," as claim 51 recites (emphasis added). Accordingly, withdrawal of the rejection is solicited.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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APPENDIX A

39. (Twice Amended) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished metal layer formed over said substrate, said electro-mechanically polished metal layer [having a reduced number of cavities and/or scratches] containing no hardening additive.

43. (Three Times Amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished surface [, said electro-mechanically polished surface having a reduced number of cavities and/or scratches] containing no hardening additive.

48. (Twice Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer provided over said substrate [, wherein said electro-mechanically polished layer has a reduced number of cavities and/or scratches] containing no hardening additive.

49. (Amended) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished [noble] metal layer consisting of a noble metal formed over said substrate.

50. (Amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished [noble] metal surface consisting of a noble metal.

51. (Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished [noble] metal layer consisting of a noble metal provided over said substrate.